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EL896635543US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Daniel Yap, et al.)
Serial No.: Not yet assigned) Group: unknown
Filed: concurrently herewith) Examiner: unknown
For: "PRECISION ELECTROPLATED SOLDER)
BUMPS AND METHOD FOR) Our Ref: B-3752DIV 619413-2
MANUFACTURING THEREOF") Date: January 15, 2002

J1017 U.S. PRO
10/05/2002
01/15/02

Box New Patent Application
Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

In accordance with the Applicants' duty to disclose information which may be material to the examination of this application, the undersigned respectfully requests that the documents cited by the Examiner and/or submitted by the Applicants in connection with U.S. Serial No. 09/522,803 filed on March 9, 2001 (the parent of Applicants' subject application) be considered when the subject application is examined.

For the Examiner's convenience, Form PTO-1449 (modified) is enclosed herewith listing the documents cited by the Examiner in connection with U.S. Serial No. 09/522,803. A copy of the cited documents can be found in the parent application, U.S. Serial No. 09/522,803.

The filing of this Information Disclosure Statement shall not be construed as a representation that a search has been made (37 C.F.R. 1.97(g)), an admission that the information cited is, or is considered to be, material to patentability, or that no other material information exists.

The filing of this Information Disclosure Statement shall not be construed as an admission against interest in any manner. (Notice of January 9, 1992, 1135 O.G. 13-25, at 25.)

Information Disclosure Statement
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The person making this statement is the practitioner who signs below on the basis of information supplied by an individual associated with the filing and prosecution of this application (37 C.F.R. § 1.56(c)) and on the basis of information in the practitioner's file.

The Commissioner is authorized to charge any additional fees which may be required or credit overpayment to deposit account no. 12-0415. In accordance with 37 CFR 1.97(b)(1), no fees should be due because this IDS is being filed concurrently herewith.

Respectfully submitted,



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Enclosures: Form PTO-1449 (modified) (1 page)

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Form PTO-1449 (Modified)	ATTY DOCKET NO. B-3752DIV 619413-2	U.S. SERIAL NO. Not yet assigned
LIST OF PATENTS AND PUBLICATIONS STATEMENT	APPLICANT Daniel Yap, et al.	
	FILING DATE concurrently herewith	GROUP unknown

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	ISSUE DATE	NAME	CLASS	SUB-CLASS	FILING DATE OR 102(e) DATE IF APPROPRIATE
	3,663,184	5/1972	Wood, et al.			
	4,661,375	4/1987	Thomas			
	5,492,235	2/1996	Crafts, et al.			
	5,763,456	4/1998	Akram			
	5,767,010	6/1998	Mis, et al.			
	5,773,359	6/1998	Mitchell, et al.			
	6,133,136	10/2000	Edelstien			
	5,162,257	11/1992	Yung			9/1991
	5,376,584	12/1994	Agarwala			12/1992
	5,480,835	1/1996	Carney, et al.			12/1994
	5,767,010	6/1998	Mis, et al.			11/1996

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	PUBLICATION DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES/NO
	JP-61225839-A	10/1986	JPO			

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	Imler, W.R., "Precision Flip-Chip Solder Bump Interconnects for Optical Packaging," <i>IEEE Transactions on Components, Hybrids, and Manufacturing Technology</i> , Vol. 15, no. 6 (Dec. 1992), Pp. 977-981.
	Kawanobe, T., et al., "Solder Bump Fabrication by Electrochemical Method for Flip Chip Interconnection," <i>IEEE</i> , Publication CH1671-7/0000 (1981), pp. 149-155.
	Yung, E.K., et al. "Flip-chip Process Utilizing Electroplated Solder Joints," MCNC Technical Report TR90-43, October 1990.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.